REMARKS

I. Introduction

In response to the Office Action dated November 2, 2005, claims 1-13, 17, 18-28, and 33-53 have been amended. Claims 1-53 remain in the application. Re-examination and re-consideration of the application, as amended, is requested.

II. Examiner Interview

Reference is made to telephonic interviews between the Applicants' attorney, Victor G. Cooper, and Examiner Ngo on February 1, 2006, and March 2, 2006, in which the relationship between the references of record and the claims, and the meaning of "holding" were discussed.

III. Claim Amendments

Applicants' attorney has made amendments to the claims as indicated above to clarify the scope of the Applicants' invention.

IV. Non-Art Rejections

In paragraph (1), the Office Action rejected claims 1-13, 15, 16, 17-28, 30, 31, and 33-35 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

According to the Office Action, claims 1, 18, 33, 37, and 47 are indefinite because they do not specify what is being bypassed by the "bypass" input. The foregoing amendments clarify the this issue.

The Office Action also rejects claims 1, 15, 16, 18, 30, 31, 33, 37 and 45 as indefinite because the claims do not define whether "to hold a value" means "store" a value, to "stop it from transmitting," or both.

The Applicants respectfully traverse. To "hold an input value" means just that ... the input is held to a value. The Applicants respectfully point out that the law does not require the Applicant to recite *how* the value is held in the claim. MPEP § 2173.04 recites:

> Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.

Nonetheless, for purposes of explanation, the Examiner is invited to consider the following remarks:

Holding: The Examiner has asked whether the "holding" operation requires "storing". As described in the Applicants' specification, "holding" can be accomplished using a number of techniques. Whether such techniques involve "storing" or not depends on the Examiner's definition of "storing".

The Applicants' disclosure presents at least two ways in which an input value can be held. One technique is to store the value in a latch coupled to the input and to prevent the value from changing. This certainly involves "storage" as the input value is stored in the latch. Another disclosed technique is to use logic to regenerate an input value by feeding back appropriate signals that derive from the signals that are output from the circuit itself. Such circuits are also known as "sequential circuits".

In a sequential circuit, the output is not just a function of the input ... it is also a function of the *previous* output values. Given this characteristic, it may be said that sequential circuits possess some form of memory; since the circuit must know, at the time a new input arrives, what the previous output was, and the circuit's response to the new input must be influenced by the previous output state as well as by the input.

Just as the simplest of memory circuits, the classical circular interconnection of two inverters shown in Fig. 1 below, employs *feedback*, it is crucial that feedback be present in a sequential logic circuit. (See such circuits as defined, for example, on p. 14 of the textbook, *Contemporary Logic Design*, by Katz described below.)

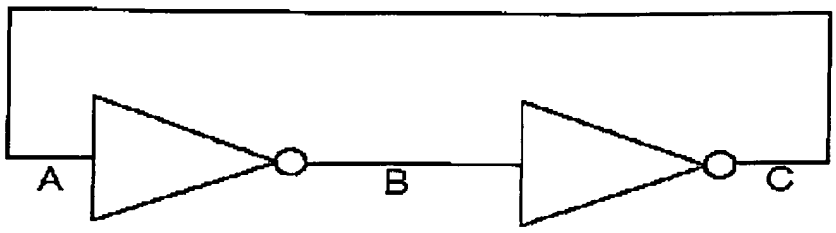

Fig. 1. Simple memory cell made with two inverters.

The feedback configuration shown in Fig. 1 provides the capability to *hold* whatever value might have been imposed on node A. If A = 1, then B = 0, which causes C = 1, and the feedback from C to A holds A at the value 1. If, however, A = 0, then B = 1, which causes C = 0, and the feedback from C to A holds A at the value 0. This is analogous to the *holding* capability that some embodiments of the Applicants' invention impose (conditionally) upon an adder circuit. That such input-holding via feedback can be done in more interesting circuits (i.e., more interesting than just the pair-of-inverters loop of Fig. 1)—circuits such as an adder (e.g., the circuit of FIG. 25A)—was heretofore unknown.

For example, FIG. 25A of the Applicants' specification describes an embodiment in which logic is used to *regenerate* an input value by feeding back appropriate signals (e.g., signal 2554) that derive from signals that are output from the adder circuit itself. The *input value* is "held" because the *input value* does not change as a result of this feedback.

Is the regeneration of the input value from the output "storing"? Page 16 of the textbook, *Contemporary Logic Design*, Benjamin/Cummings, 1992, (written by Dr. R. H. Katz, a professor at University of California, Berkeley), defines "storage elements" as "primitive sequential networks that can either hold their current values or allow them to be replaced."

To the extent that the regenerative embodiments of the Applicants' invention, are *sequential* circuits and they possess the property that they "can either hold their current values or allow them to be replaced," such circuits may be considered to be performing a

"storing" operation.[1] (In FIG. 25A, the "holding or replacing" is evident for the previously indicated signal 2554 of FIG. 25A, wherein the absence of the *bypass* input signal causes the feedback to be interrupted and causes the input signal value to be replaced by whatever signal value is then appearing at input B.)

The regenerative embodiments may therefore be said to possess the attribute of storage. However, the key is not that they store the input value nor how that input value is stored ... it is that they *hold* the input value ... whether implemented by regeneration or by a straightforward storage element , or other means (recall the Applicants also describe and claim some embodiments in which a *latch*, a quintessential *storage* element, is employed --- see, e.g., Figs. 33 and 34 --- along with combinational logic elements).

So, depending on the Examiner's definition of the term, the Applicants' regenerative embodiments may also be said to involve "storage". However, the key characteristic of the Applicants' invention remains "holding" the value of the input, not storage.

Finally, regarding the matter of "stopping or preventing transmitting": Embodiments of the Applicants' invention do employ elements that perform this function (e.g. by passing only one of a plurality of inputs, those not passed are prevented from being transmitted). Our specification also describes the use of transmission gates, and "stopping or preventing transmitting" is essentially what transmission gates do. In the previously referenced Fig. 25A, for example, transmission gate 2524 can "stop or prevent the transmitting of" input signal B, and transmission gate 2552 can "stop or prevent the transmitting of" the regenerated signal that, when allowed to pass, provides—and holds the value of—the new input signal B.

Applicants have amended claims 1-13, 17, 18-28, and 33-53 to recite both the "holding" and "passing only one" features. The Applicants believe that these changes render the meaning of these claims clear and distinguishable from the prior art of record.

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[1] Some of the embodiments of the Applicants' disclosure also simultaneously perform other functions (e.g., perform as adders) so, in this sense they are perhaps not correctly referred to as "*primitive* ..." (as in the above Katz definition), but then we have not referred to our circuits as being "storage elements."

V. The Cited References and the Subject Invention

A. The Smith Jr. Reference

U.S. Patent No. 3,482,085, issued December 2, 1969 to Smith Jr., discloses a binary full adder-subtractor with bypass control. The bypass control has the effect of suppressing the arithmetic operation of the adder-subtractor and causing one of the arguments to the operation to be produced at the output; however, the borrow or carry signal is still produced as if the operation had not been suppressed. The bypass control might be generated, for example, when a negative difference would be produced by the suppressed operation. The adder-subtractor has particular application in matrix arithmetic units capable of the more complex arithmetic operations of multiply, divide, root taking, power generation, etc., and is preferably constructed of semiconductor logic circuits.

VI. Office Action Prior Art Rejections

In paragraph (2), the Office Action rejected claims 14, 17, 29, and 32 under 35 U.S.C. § 102(b) as being clearly anticipated by Smith Jr., U.S. Patent No. 3,482,085 (Smith). Applicants respectfully traverse these rejections.

According to the Office Action, FIG. 1 of the Smith reference teaches:

> "an adder for adding first input (E) a second input (P), and a carry input (F) to produce an adder output (T) and a carry output (G). The adder also has a bypass input (K) for controlling the logic of the adder to generate an adder output and a carry output as claimed (suppressing the arithmetic operations of the adder see abstract and col. 5, lines 40-71)"

It is important to distinguish between the suppression of the *arithmetic* operation and the suppression of the *computational* operations involved with performing the arithmetic operation (e.g., addition). As explained above, our circuit suppresses the actual computational operations when the bypass signal is applied. Smith, however, teaches a system that suppresses simply the *arithmetic operation* of addition. (Indeed, to quote the Smith Abstract, it just has "the *effect* of suppressing the arithmetic operation.") Smith does not claim that his circuit does not *do* the addition; in fact the Smith circuit may perform the addition/subtraction operation even when it is in bypass mode.) As a consequence, the Smith circuit achieves the bypassing of the adder only in a "logical"

sense. It provides one of the input signals at the Sum output, and in doing so it causes the effect of "no addition" in the arithmetic result—as if the adder had been bypassed. But the Smith circuit does this without suppressing the *computational* operations within the adder. Those *are not suppressed* and hence, regardless of whether the bypass signal is ON or OFF, the Smith system performs computations to produce the Sum output.

Unlike our bypassable adder, power is dissipated within the Smith adder's logic gates even when "bypassing" is occurring. Smith simply performs "logical bypassing." In fact, a close reading of the details of the Smith patent specification will show that even *more* power can be burned (because even more computation can be performed) by the Smith bypassable adder when it is in "bypassing mode" than the amount of power it burns when it is in "normal adder" mode! In our claims 14, 17, 29, and 32 we refer to providing the output without *computing* the output and this feature distinguishes our circuit's operation from circuits such as Smith's where computing occurs even when the effect of bypassing is being produced.

It should be noted that Smith's circuits possess neither the "holding" or the "storage" attributes of the Applicant's invention. By inspection, Smith recalculates values within the adder ... it does not hold the input value to prevent such recalculation. In fact, Smith's circuits *cannot* possess storage capabilities because they disclose only *combinational* circuits ... the input value is not regenerated, nor is a separate memory element (such as a latch) used.

In summary, in Smith's circuit, the system's output may have the same *value* as one of its inputs, but the value of its final output result is obtained according to a process in which substantial *computing* is performed. In our system, as stated in Claims 14, 17, 29, and 32, the computing is not performed (and hence power is saved).

VII. Dependent Claims

Dependent claims 2-13, 15-17, 19-28, 30-32, 34-36, 37-44, and 46-53 incorporate the limitations of their related independent claims, and are therefore patentable on this basis. In addition, these claims recite novel elements even more remote from the cited references. Accordingly, the Applicants respectfully request that these claims be allowed as well.

VIII. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

GATES & COOPER LLP
Attorneys for Applicant(s)

Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045
(310) 641-8797

Date: March 2, 2006

By: _____
Name: Victor G. Cooper
Reg. No.: 39,641

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